AK

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,817	08/29/2001	Cindy Seibel	3521.150	7575

7590 07/18/2003

PETERS, VERNY, JONES & BIKSA LLP
ATTORNEYS AT LAW
SUITE 6
385 SHERMAN AVENUE
PALO ALTO, CA 94306-1827

EXAMINER	
. HOGANS, DAVID L	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,817	SEIBEL ET AL.	
	Examiner	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to Amendment B filed on May 1, 2003.

Status of Claims

Claims 1-23 are pending.

Claim Objections

1. Claim 1 is objected to because of the following informalities: line 10 contains duplicate words "to heat said top surface layer". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3 and 8-10 are rejected under 35 U.S.C. 102(e) as being anticipated by 6,391,731 to Chong et al.

In reference to Claims 1-3 and 8-10, Chong et al. teaches:

- forming a MOS doped polycrystalline silicon gate on a crystalline silicon substrate (10) (See Figures 1-11 and columns 2-5 lines 35-40)
- forming an insulation layer comprised by silicon dioxide (18) on said top surface of the silicon substrate (10) (See Figures 1-11 and columns 2-5 lines 35-40)

- forming an amorphous silicon layer (34) on top of and in contact with said insulation layer (18) (noting that Chong et al. teaches that by carefully selecting the weight of the ion, the implantation dose and the implantation energy, the depth of the amorphous layer can be controlled; further noting that the gate thickness is between 500-2500 angstroms and that the amorphous layer implantation depth is between 300-1500 angstroms) (See Figures 1-11 and columns 2-5 lines 35-40 – noting especially column 3 lines 35-55)
- introducing a dopant (50) in a top surface layer of said amorphous silicon layer via implantation of of B+, BF_2+, As+ or P+ (See Figures 1-11 and columns 2-5 lines 35-40)
- irradiating said top surface of said amorphous silicon layer with a laser beam (100) to heat said top surface layer between 1150°C (the known approximate melting temperature of amorphous silicon) and the melting temperature of said silicon substrate to cause explosive recrystallization of said amorphous layer into a polycrystalline silicon gate with said dopant distributed uniformly (See Figures 1-11 and columns 2-5 lines 35-40)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,391,731 to Chong et al. in view of 6,274,488 to Talwar et al.

Incorporating all arguments of Claims 1 and 3 and noting that Chong et al. teaches a laser with a wavelength of 157-308 nanometers and a fluence of 0.1-1.5 J/cm^2 but fails to teach a pulse width of less than 1 ms, a repetition rate between 200-400 Hz and 3-10 pulses.

However, Talwar et al., in column 6 lines 08-33, teaches a pulsed laser comprising between 3 and 10 pulses, with a pulse width of less than 1 ms and a repetition rate between 200-400 Hz.

It would have been obvious one of ordinary skill in the art to modify Chong et al. by incorporating a pulsed laser comprising between 3 and 10 pulses, with a pulse width of less than 1 ms and a repetition rate between 200-400 Hz, as taught by Talwar et al., because radiation beams operating within these process margins are absorbed by amorphous silicon and not by crystalline silicon.

6. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,391,731 to Chong et al. in view of 6,159,782 to Xiang et al. in view of Microchip Fabrication – A practical guide to Semiconductor Processing (2000) to Van Zant.

Claim 6

Incorporating all arguments of Claim 1 and noting that Chong et al. fails to explicitly teach depositing a metal contact atop the polycrystalline gate.

However, Xiang et al., in columns 8-9 lines 63-30, teaches depositing a metal contact atop the polycrystalline gate.

It would have been obvious to one of ordinary skill in the art to modify Chong et al. by incorporating a metal contact atop the polycrystalline gate, as taught by Xiang et al., to lower the effective gate resistance.

Claim 7

Incorporating all arguments of Claims 1 and 6 and noting that Chong et al. and Xiang et al. fail to explicitly teach wherein the metal contact is comprised by at least one of tungsten, tungsten silicide, tungsten nitride, tantalum, tantalum nitride, titanium, titanium nitride or platinum.

However, Van Zant, on pages 403-404, teaches wherein modern day circuit design, especially MOS circuits, employ refractory metals (titanium, tungsten and tantalum) or their silicides as conductive layers due to their lower resistivity and lower contact resistance.

It would have been obvious to one of ordinary skill in the art to modify Chong et al. and Xiang et al by incorporating a metal contact comprised by at least one of tungsten, tungsten silicide, tantalum or titanium, as taught by Van Zant, to produce a contact with a lower resistance value.

7. Claims 11, 15 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,391,731 to Chong et al. in view of 5,966,605 to Ishida.

Chong et al. teaches forming a MOS doped polycrystalline silicon gate on a crystalline silicon substrate (10) (See Figures 1-11 and columns 2-5 lines 35-40); forming an insulation layer comprised by silicon dioxide (18) on said top surface of the silicon substrate (10) (See Figures 1-11 and columns 2-5 lines 35-40); forming an amorphous silicon layer (34) on top of and in contact with said insulation layer (18) (noting that Chong et al. teaches that by carefully selecting the weight of the ion, the implantation dose and the implantation energy, the depth of the amorphous layer can be controlled; further noting that the gate thickness is between 500-2500 angstroms and that the amorphous layer implantation depth is between 300-1500 angstroms) (See Figures 1-11 and columns 2-5 lines 35-40 – noting especially column 3 lines 35-55); introducing a dopant (50) in a top surface layer of said amorphous silicon layer via implantation of of B+, BF_2+, As+ or P+ (See Figures 1-11 and columns 2-5 lines 35-40); irradiating said top surface of said amorphous silicon layer with a laser beam (100) to heat said top surface layer between 1150°C (the known approximate melting

temperature of amorphous silicon) and the melting temperature of said silicon substrate to cause explosive recrystallization of said amorphous layer into a polycrystalline silicon gate with said dopant distributed uniformly (See Figures 1-11 and columns 2-5 lines 35-40).

Chong et al. fails to explicitly teach forming a dopant layer on top of and in contact with said amorphous silicon layer.

However, Ishida, in column 4 lines 25-35, teaches forming a dopant layer over a silicon surface by projection gas immersion doping.

It would have been obvious to one of ordinary skill in the art to modify Chong et al. by incorporating the formation of a dopant layer over a silicon gate by projection gas immersion doping, as taught by Ishida, as an alternative to doping the silicon gate by ion implantation.

8. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,391,731 to Chong et al. in view of 5,966,605 to Ishida in view of Microchip Fabrication – A practical guide to Semiconductor Processing (2000) to Van Zant.

Incorporating all arguments of Claim 11 and noting that Chong et al. and Ishida teach a dopant layer formed by chemical vapor deposition (See Ishida column 4 lines 25-35) but fail to explicitly teach a dopant layer formed by sputtering or evaporation.

However, Van Zant, on page 411, teaches that sputtering and evaporation are known and conventional within the art for vacuum deposited materials. Furthermore, sputtering offers the advantage of deposition of the dopant without chemical or compositional change of the dopant and evaporation deposits low energy atoms without damage to the surface substrate.

It would have been obvious to one of ordinary skill in the art to modify Chong et al. and Ishida by incorporating a deposited film formed by sputtering or evaporation, as taught by Van Zant, because such techniques are known and conventional within the art for vacuum deposited materials.

9. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,391,731 to Chong et al. in view of 5,966,605 to Ishida in view of 6,274,488 to Talwar et al.

Incorporating all arguments of Claims 11 and 15 and noting that Chong et al. teaches a laser with a wavelength of 157-308 nanometers and a fluence of 0.1-1.5

J/cm^2 but fails to teach a pulse width of less than 1 ms, a repetition rate between 200-400 Hz and 3-10 pulses.

However, Talwar et al., in column 6 lines 08-33, teaches a pulsed laser comprising between 3 and 10 pulses, with a pulse width of less than 1 ms and a repetition rate between 200-400 Hz.

It would have been obvious one of ordinary skill in the art to modify Chong et al. and Ishida by incorporating a pulsed laser comprising between 3 and 10 pulses, with a pulse width of less than 1 ms and a repetition rate between 200-400 Hz, as taught by Talwar et al., because radiation beams operating within these process margins are absorbed by amorphous silicon and not by crystalline silicon.

10. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,391,731 to Chong et al. in view of 5,966,605 to Ishida in view of 6,159,782 to Xiang et al. in view of Microchip Fabrication – A practical guide to Semiconductor Processing (2000) to Van Zant.

Claim 18

Incorporating all arguments of Claim 11 and noting that Chong et al. and Ishida fail to explicitly teach depositing a metal contact atop the polycrystalline gate.

However, Xiang et al., in columns 8-9 lines 63-30, teaches depositing a metal contact atop the polycrystalline gate.

It would have been obvious to one of ordinary skill in the art to modify Chong et al. and Ishida by incorporating a metal contact atop the polycrystalline gate, as taught by Xiang et al., to lower the effective gate resistance.

Claim 19

Incorporating all arguments of Claims 11 and 18 and noting that Chong et al., Ishida and Xiang et al. fail to explicitly teach wherein the metal contact is comprised by at least one of tungsten, tungsten silicide, tungsten nitride, tantalum, tantalum nitride, titanium, titanium nitride or platinum.

However, Van Zant, on pages 403-404, teaches wherein modern day circuit design, especially MOS circuits, employ refractory metals (titanium, tungsten and tantalum) or their silicides as conductive layers due to their lower resistivity and lower contact resistance.

It would have been obvious to one of ordinary skill in the art to modify Chong et al., Ishida and Xiang et al by incorporating a metal contact comprised by at least one of tungsten, tungsten silicide, tantalum or titanium, as taught by Van Zant, to produce a contact with a lower resistance value.

11. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over 6,391,731 to Chong et al. in view of 5,966,605 to Ishida further in view of 6,077,758 to Zhang et al.

Incorporating all arguments of Claim 11 above and noting that Chong et al. and Ishida fail to explicitly teach dopant concentrations of at least one of boron, arsenic and phosphorus up to $3x10^{20}$ ions/cm^3, $5x10^{20}$ ions/cm^3, and $1x10^{21}$ ions/cm^3, respectively.

However, Zhang et al., in column 10 lines 51-55, teaches a doping concentration of phosphorus or boron between 10^{19} and 10^{21} cm^{-3}. Examiner notes that it is known and conventional within the art to dope silicon with boron or phosphorus at concentration levels of 10^{19} to 10^{21} ions/cm^{-3}, to reduce or lower resistivity.

It would have been obvious to one of ordinary skill in the art to modify Chong et al. and Ishida by incorporating the above doping concentrations, as taught by Zhang et al., to lower the resistivity of the device.

Response to Arguments

11. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,387,784 to Chong et al. teaches laser annealing a doped amorphous silicon layer to initiate recrystallization.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (703) 305-3361. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

dh
July 11, 2003

Carl Whitehead

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800